What is Claimed:

1. An integrated circuit comprising:

a substrate;

a plurality of bond pads formed above the substrate; and

a first conductive region formed at an outer region of the substrate and coupled to at least two of the plurality of bond pads.

2. The integrated circuit of claim 1 wherein the first conductive region surrounds the plurality of bond pads.

3. The integrated circuit of claim 2 wherein the first conductive region has a chamfered region.

4. The integrated circuit of claim 1 further comprising:

second conductive regions adapted to interconnect devices formed in the integrated circuit,

wherein the first conductive region is separate from the devices.

5. The integrated circuit of claim 1 wherein the first conductive region comprises at least two separate first conductive regions.

6. The integrated circuit according to claim 5 wherein the at least two separate first conductive regions have a varying height relative to an upper surface of the substrate.

7. The integrated circuit according to claim 1 wherein the first conductive region is formed at the periphery of the integrated circuit.

8. The integrated circuit of claim 1 wherein the first conductive region comprises at least two separate conductive regions, each of the separate conductive regions coupled to at least two of the plurality of bond pads.

9. A test system adapted to test the integrated circuit of claim 1 comprising:

a tester configured to test an electrical characteristic of the first region via the at least two bond pads.

10. An integrated circuit comprising:

a substrate;

a plurality of bond pads; and

a conductive runner formed on the substrate and around the plurality of bond pads, the conductive runner electrically coupled to at least two of the plurality of bond pads.

11. The integrated circuit of claim 10 further comprising a plurality of the conductive runners.

12. The integrated circuit according to claim 11 wherein at least two of the plurality of the conductive runners a varying height relative to an upper surface of the substrate.

13. The integrated circuit of claim 10 wherein the conductive runner has a chamfered region.

14. The integrated circuit of claim 10 further comprising:

devices formed on the integrated circuit; and

circuit conductive runners adapted to interconnect the devices to form a circuit;

wherein the conductive runners are separate from the devices.

15. A method of manufacturing an integrated circuit including the steps of:

forming at least two bond pads above a substrate;

forming a conductive region above and at a region positioned between the at least two bond pads and an outer edge of the substrate; and

electrically coupling the bond pads to the conductive region, the conductive region not electrically coupled to devices formed on the substrate.